Wide VIN 60V Non-synchronous Boost Current Sink

1 Features

- 3.0V to 60V Wide Input Voltage
- Integrated 250mΩ 60V Power MOSFET
- 1.2MHz Fixed Switching Frequency
- Up to 95% Step-up conversion efficiency
- 1mA Light load model efficiency up to 80%
- Low than 0.1mA static current
- Low than 10uA Shutdown current
- Built-in Cycle-by-cycle current limiting
- Built-in thermal shutdown protection
- Built-in under-voltage protection
- Built-in loop compensation
- Built-in soft start circuit
- Simple external circuit
- Available in a SOT-235 or ESOP8 package

2 Applications

- Digital Set-top Box (STB)
- Tablet Personal Computer (Pad)
- LCD Bias Supply
- Battery-Powered Equipment
- Portable Media Player (PMP)
- General Purposes

2 General Description

The ZCC6302 is a constant frequency, mode step-up converter intended for small, low power applications. The ZCC6302 switches at 1.2MHz and allows the use of tiny, low cost capacitors and inductors 5mm or less in height. Internal soft-start results in small inrush current and extends battery life.

The ZCC6302 includes under-voltage lockout, current limiting, and thermal overload protection to prevent damage in the event of an output overload. The ZCC6302 is available in a small SOT-23 or ESOP8 package.

4 Typical Application

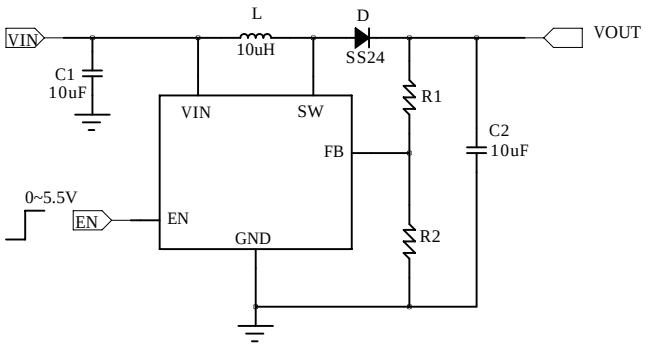


Figure1. Basic Application Circuit

5 PIN description

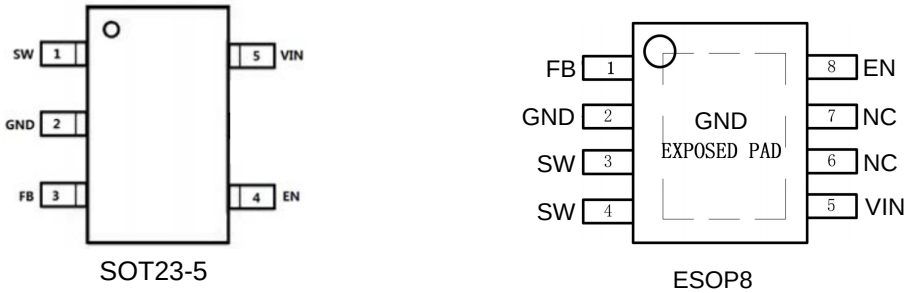


Figure 1 Packge Pinout

PIN Functions

PIN			I/O	DESCRIPTION
NAME	SOT23-5	ESOP8		
SW	1	3、4	PWR	Boost switch output, connect 10uH inductor
GND	2	2、EXP	GND	System ground pin
FB	3	1	I	Voltage feedback input. The control loop will regulation this pin to 1.2V
EN	4	8	I	Boost enable
NC		6、7	NC	NC pin.
VIN	5	5	PWR	Input voltage bias

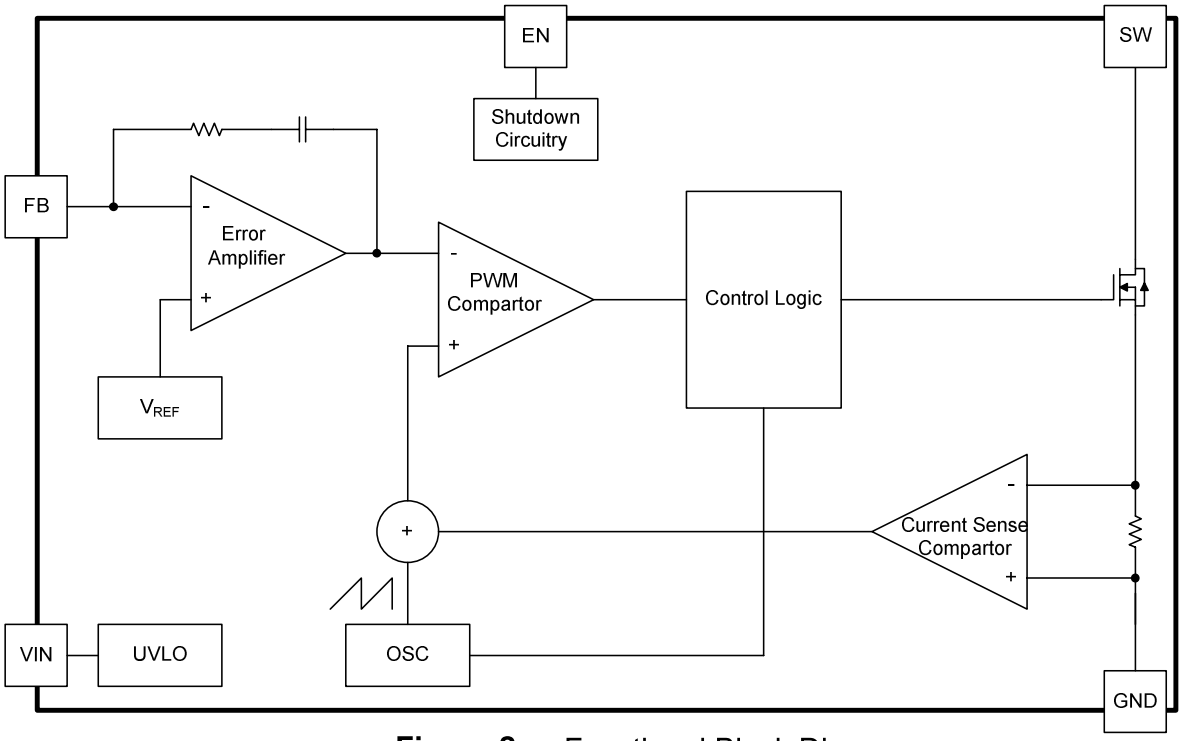


Figure 2. Functional Block Diagram

6 Specifications

6.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
Voltage range at terminals	VIN, SW	-0.3	65	V
Voltage range at terminals	FB, EN	-0.3	6	V
Current range at terminals	SW	0	3	A
Operating junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	°C

6.2 ESD Ratings

		MAX	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM) ESD stress voltage	±2000	V
	Charged device model (CDM) ESD stress voltage	±1000	V

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{SYSIN}	Input voltage range	3.0		60	V
V_{OUTD}	Boost converter output voltage range	VIN*1.1		60	V
L	Effective inductance range	2.2	10		μH
C_{IN}	Input effective capacitance range	2.2	4.7		μF
C_{OUT}	Output effective capacitance range	4.7	10	100	μF
T_J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		ZCC6302	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	220	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	110	°C/W

6.5 Electrical Characteristics

T_J = -40°C to 125°C and V_{IN} = 3.3V to 60V. Typical values are at V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Boost						
V_{IN}	Input voltage range		3.0		60	V
V_{UVLO}	Under voltage lockout threshold	V_{SYSIN} rising		3.0		V
		V_{SYSIN} falling		2.7		V
V_{IN_HYS}	VIN UVLO hysteresis			0.5		V
F_{SW}	Boost switch frequency	V_{IN}=12V, EN = hi	1.1	1.2	1.3	MHz
F_{SW_FB}	Boost switch fold back frequency	V_{IN}=12V, EN = hi		300		KHz
R_{hs}	Low side FET on resistor	V_{SYSIN}=12V		250		mΩ
I_{LIM}	Switch current limit	V_{OUT} ≥ 3V, boost operation	1.6	2		A
Iq	Operation current with no switch	EN= 1, FB = 2V		120		uA
Isd	Shut down current	EN= 0, VIN= 12V		10	20	uA
D_{MAX}	Maximum duty cycle		89	91		%
I_{SW}	SW leakage current	V_{SYSIN}=12V, V_{OUTD} = 3.3V			<4	uA
V_{FB}	FBU feedback voltage		1.195	1.2	1.205	V
I_{FBU}	FBU leakage current				50	nA
V_{ENH}	EN Threshold, Rising				0.6	V
V_{ENL}	EN Threshold, Rising		0.3			V
V_{EN_min}	EN minimal analog dimming voltage			0.6		V
V_{EN_max}	EN minimal analog dimming voltage			1.2		V
I_{EN_LKG}	EN input current	V_{EN} = 5V		6.5		uA
T_{on_min}	EN input minimal on time		20			us
F_{req_Ddim}			50			KHz
T_{sd}	Overtemperature protection			150		°C
T_{sd_hyst}	Overtemperature hysteresis			30		°C

8 Functional Description

The ZCC6302 uses a fixed frequency, peak current mode boost regulator architecture to regulate voltage at the feedback pin. The operation of the ZCC6302 can be understood by referring to the block diagram of Figure 2. At the start of each oscillator cycle the MOSFET is turned on through the control circuitry. To prevent sub-harmonic oscillations at duty cycles greater than 50 percent, a stabilizing ramp is added to the output of the current sense amplifier and the result is fed into the negative input of the PWM comparator. When this voltage equals The output voltage of the error amplifier the power MOSFET is turned off. The voltage at the output of the error amplifier is an amplified version of the difference between the 1.2V band gap reference voltage and the feedback voltage. In this way the peak current level keeps the output in regulation. If the feedback voltage starts to drop, the output of the error amplifier increases. These results in more current to flow through the power MOSFET, thus increasing the power delivered to the output. The ZCC6302 has internal soft start to limit the amount of input current at startup and to also limit the amount of overshoot on the output.

Setting the Output Voltage

ZCC6302 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} * (\frac{R1}{R2} + 1)$$

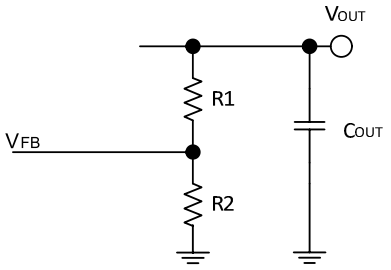


Figure3. Setting the Output Voltage

Inductor Selection

The ZCC6302 boost converter can utilize small surface mount and chip inductors due to the fast 1.2MHz switching frequency. Inductor values between 2.2μH and 47μH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10μH will increase size while providing little improvement in output current capability. The minimum boost inductance value is given by:

$$L > \frac{V_{IN} * (V_{OUT} + V_{DIODE} - V_{IN})}{F_S * I_{RIPPLE} * (V_{OUT} + V_{DIODE})}$$

Where
• IRIPPLE：Peak-to-Peak inductor current
• VIN：Input voltage
• VOUT：Output voltage
•VDIODE：Output diode Forward Voltage
• FS：Switching frequency, Hertz

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DCR(series resistance of the winding) to reduce the I2R power losses, and must not saturate at peak inductor current levels. Molded chokes and some chip inductors usually

Capacitor Selection

The internal loop compensation of the ZCC6302 boost converter is designed to be stable with output capacitor values of 10μF or greater. Low ESR (equivalent series resistance)capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have extremely low ESR and are available in small footprints . A 10μF to 47μF output capacitor is sufficient for most fixed frequency applications. For applications where Burst Mode operation is enabled, a minimum value of 22μF is recommended. Larger values may be used to obtain very low output ripple and to improve transient response. X5R and X7R dielectric materials are preferred for their ability to maintain capacitance over wide voltage and temperature ranges. Y5V types should not be used. Case sizes smaller than 0805 are not recommended due to their increased DC bias effect.

Low ESR input capacitors reduce input switching noise and reduce the peak current drawn from the battery. It follows that ceramic capacitors are also a good choice for input decoupling and should be located as close as possible to the device. A 22μF input capacitor connected to inductor is sufficient for most applications. Larger values maybe used without limitations. For applications where the power source is more than a few inches away, a larger bulk decoupling capacitor is recommended on the input to the boost converter.

Diode Selection

A Schottky diode should be used for the output diode. The forward current rating of the diode should be higher than the load current, and the reverse voltage rating must be higher than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

Layout Consideration

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. Minimize area of switched current loops. In a boost regulator there are two loops where currents are switched rapidly. The

first loop starts from the CIN input capacitor, to the regulator VIN terminal, to the regulator SW terminal, to the inductor then out to the output capacitor COUT and load. The second loop starts from the output capacitor ground, to the regulator GND terminals, to the inductor and then out to COUT and the load. To minimize both loop areas the input capacitor should be placed as close as possible to the VIN terminal. Grounding for both the input and output capacitors should consist of a small localized topside plane that connects to GND. The inductor should be placed as close as possible to the SW pin and output capacitor.

2. Minimize the copper area of the switch node. The SW terminals should be directly connected with a trace that runs on top side directly to the inductor. To minimize IR losses this trace should be as short as possible and with a sufficient width. However, a trace that is wider than 100 mils will increase the copper area and cause too much capacitive loading on the SW terminal. The inductors should be placed as close as possible to the SW terminals to further minimize the copper area of the switch node.

3. Have a single point ground for all device analog grounds. The ground connections for the feedback components should be connected together then routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground plane. If not properly handled, poor grounding can result in degraded load regulation or erratic switching behavior.

4. Minimize trace length to the FB terminal. The feedback trace should be routed away from the SW pin and inductor to avoid contaminating the feedback signal with switch noise.

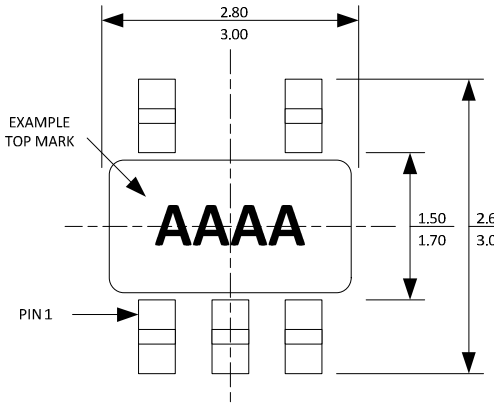
5. Make input and output bus connections as wide as possible. This reduces any voltage drops on the input or output of the converter and can improve efficiency. If voltage accuracy at the load is important make sure feedback voltage sense is made at the load. Doing so will correct for voltage drops at the load and provide the best output accuracy.

Over temperature protection

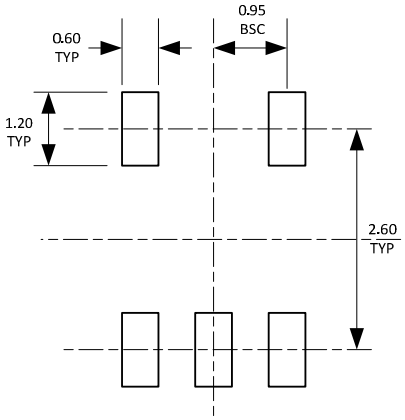
Thermal protection disables Boost when the junction temperature rises to approximately 150°C; allowing the device to cool down. When the junction temperature cools to approximately 125°C; the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

PACKAGE INFORMATION

SOT23- 5

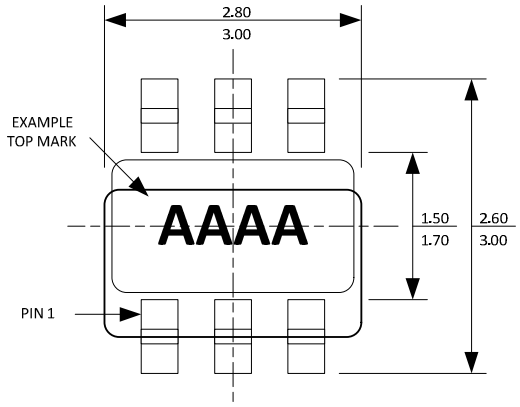


TOP VIEW

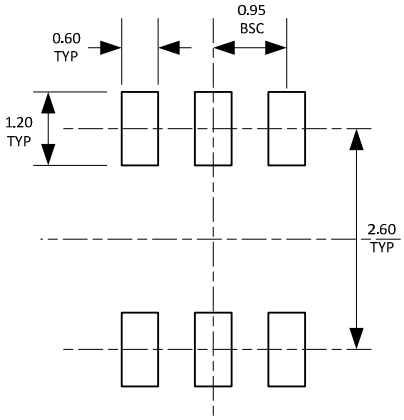


RECOMMENDED SOLDER PAD

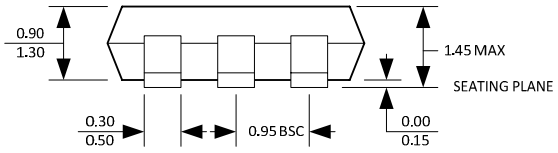
SOT23-6



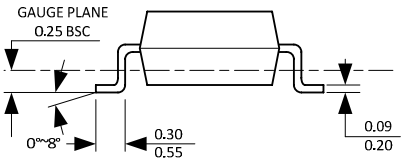
TOP VIEW



RECOMMENDED SOLDER PAD LAYOUT



FRONT VIEW

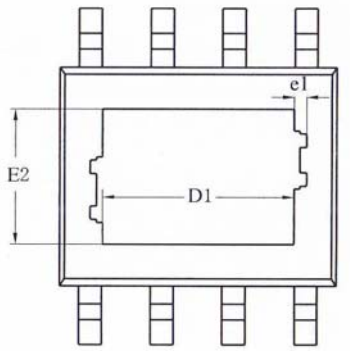


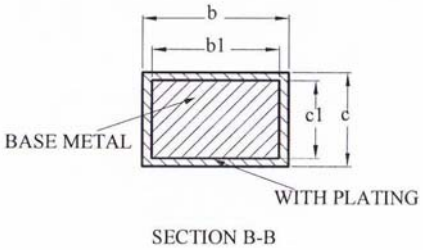
SIDE VIEW

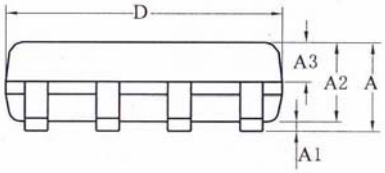
NOTE:
1.DIMENSIONS ARE IN MILLIMETERS.
2.DRAWING NOT TO SCALE.
3.DIMENSIONS ARE INCLUSIVE OF PLATING.
4.DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR.

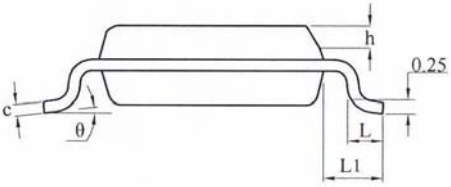
PACKAGE INFORMATION

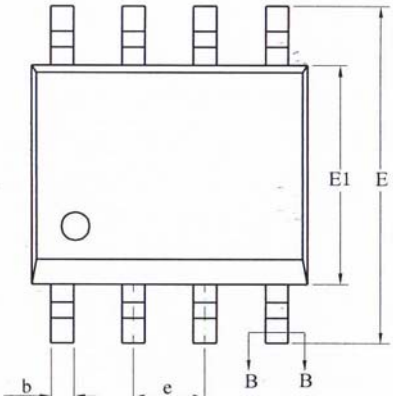
产品封装：**ESOP-8L**

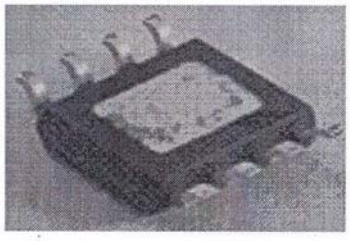












SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.65
A1	0.05	—	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	0.60	0.80
L1	1.05REF		
θ	0	—	8°

Size(mm) / L/F Size (mil)	D1	E2	e1
90*90	2.09REF	2.09REF	0.16REF
95*130	3.10REF	2.21REF	0.10REF